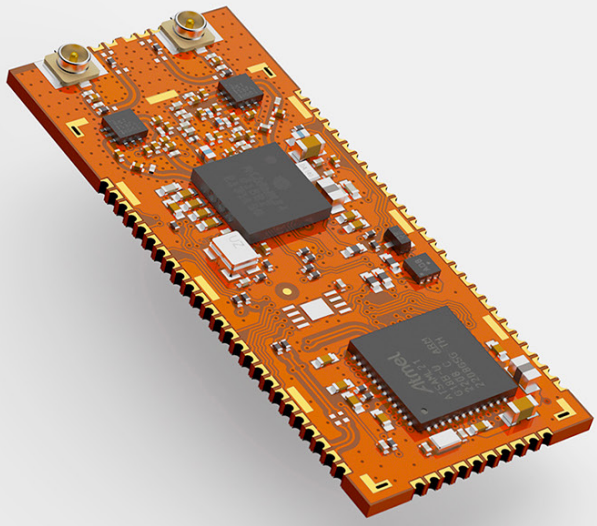
Briki MBC-LR

Long Range LoRa device



OVERVIEW

The MBC-LR, addresses to all those applications that require a device certified and optimized for very long-range, low consumption and multi-band sub-GHz Low-Power Wide-Area networks.

- From prototype to product in a simple and fast way
- Exposed debug interfaces for both the chips
- Small “1-Brick” form factor with many GPIOs
- Compatible pinout between all modules in the family
- Liquid logic to surpass the classical rigid master/slave topology
- Embedded security thanks to the dedicated cryptochip
- Software-selectable flexible power modes
- Software-selectable radio band (868MHz, 915MHz or 433MHz)

FEAUTURES

Technical information

- ATSAML21G18B ARM® Cortex®-M0+
- ATSAMR34J18B SiP featuring a ARM® Cortex®-M0+ / Semtech SX1276
- CryptoAuth ECC608A chip
- Several band configurations available: 868/915/433 MHz, Only 868, Only 915, 868+433MHz
- Opt. Antenna available on U.FL connector or Castellated Holes (for Antenna on PCB)
- Opt. Crystal for standard range, or TCXO for very long range applications

- Product size: 38 x 16 mm
- Format: 1 brick

This product is sold by request as products for industrial use. The MBC module is available in different versions by hardware configuration and functionalities. Depending on your design, you may prefer one version over the other. Contact us to find the best suited for you!

DEVELOPMENT TOOLS

Firmware and software tools

Meteca offers a complete firmware solution for both the MCUs, written in C/C++ and fully compatible with Arduino for a fast and simple prototyping process.

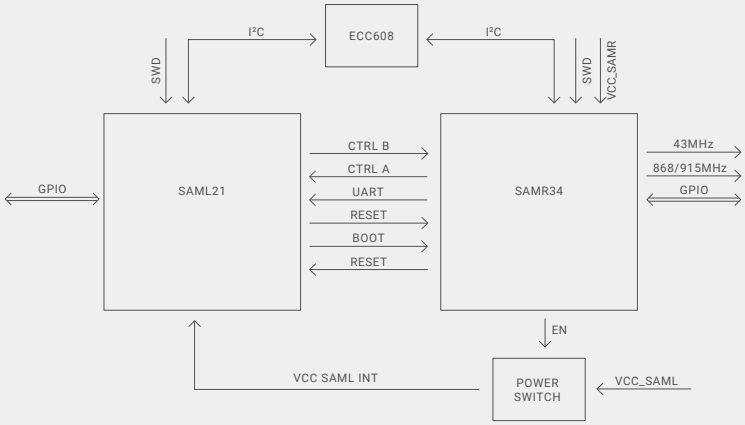
All Briki MBCs are completely programmable using the Arduino IDE or a more professional IDE like Visual Studio Code. The latter, in particular, allows customers to program both the MCUs using different programming languages and/or SDK like Microchip's ASF or python.

Both the MCUs have their debugging interface exposed on the module's pinout to ensure full control over the firmware implementation. In conjunction with Visual Studio Code, several debugging devices can be used to extensively debug the code: ATMEL ICE (link) for the ARM Cortex MCU and/or Segger J-Link (link), useful for both the MCUs.

The software suite offered includes a set of tools specifically designed to allow firmware update procedure (via USB for both the MCUs) along with automatic pin-mapping configuration.

TECH SPECS

Block diagram



SAML21

PROCESSOR

ARM©, Cortex-M0+ CPU up to 48MHz

MEMORIES

256KB in-system self-programmable Flash

32KB SRAM Memory

SYSTEM

External Interrupt Controller (EIC), 16 external interrupts, one non-maskable interrupt

LOW POWER

Idle, standby, battery backup and off sleep modes

SleepWalking peripherals

Static and dynamic power gating architecture

PERIPHERALS

16-channel Direct Mem Access Controller (DMAC)

12-channel Event System

Five configurable 16-bit Timer/Counters (TC)

Two 24-bit and one 16-bit Timer/Counters for Control (TCC)

32-bit Real Time Counter (RTC) with clock/calendar function

Watchdog Timer (WDT)

CRC-32 generator, AES encryption engine and True Random Generator

One Configurable Custom Logic (CCL)

One full-speed USB (12Mbps) Device/Host

Up to six SERCOM digital interfaces like: I²C (up to 3.4MHz), SMBUS/PMBUS, SPI, LIN, UART and analog interfaces like: 12-bit, 1Msps ADC, two 12-bit 1Msps DACs, Two Analog Comparators, 3 OPAMPS, Peripheral Touch Controller with capacitive touch and proximity sensing I/O

ATECC608A

CLOUD AUTHENTICATION

for AWS IoT and Google Cloud IoT Core

HARDWARE SECURITY FEATURES

Cryptographic coprocessor with secure key storage for up to 16 Keys, certificates or data

Asymmetric sign, verify, key agreement: ECDSA, ECDH, NIST standard P256 elliptic curve support

Support for symmetric algorithms: SHA-256 & HMAC hash including off-chip context save/restore, AES-128 with encrypt/decrypt, galois field multiply for GCM

Networking key management support

Turnkey PRF/HKDF calculation for TLS 1.2/1.3

Ephemeral key generation and key agreement in SRAM

SECURE BOOT SUPPORT

Implementation with ATSAMD21 Cortex-M0+

Full ECDSA code signature validation

Encryption/Authentication for messages to prevent on-board attacks

ADDITIONAL FEATURES

Internal high-quality FIPS 800-90 A/B/C Random Number Generator (RNG)

Two high-endurance monotonic counters

Guaranteed unique 72-bit serial number

1MHz Standard I2C interface

<150nA Sleep current

SAMR34

PROCESSOR

ARM©, Cortex-M0+ CPU up to 48MHz

MEMORIES

256KB in-system self-programmable Flash

32KB SRAM Memory

SYSTEM

External Interrupt Controller (EIC), 15 external interrupts, one non-maskable interrupt

LOW POWER

Idle and standby sleep modes

SleepWalking peripherals

Transceiverpower consumption: from 16mA in receiving up to 95mA in transmission (PA_BOOST)

RF/Analog Features

Integrated LoRa Technology Transceiver with Triband Coverage (137 MHz to 175 MHz; 410 MHz to 525 MHz; 862 MHz to 1020 MHz)

Up to 20 dBm (100 mW) Max Power (VDDA-NA>2.4 VDC)

High Sensitivity: down to -136 dBm (LoRaWAN™ protocol compliant modes); Down to -148 dBm (proprietary narrowband modes)

Up to 168 dB Maximum Link Budget

PERIPHERALS

12-channel Direct Mem Access Controller (DMAC)

12-channel Event System

Three configurable 16-bit Timer/Counters (TC)

Three 16-bit Timer/Counters for Control (TCC)

32-bit Real Time Counter (RTC) with clock/cal

Watchdog Timer (WDT)

CRC-32 generator

One full-speed USB (12Mbps) Device/Host

Up to five SERCOM digital interfaces like: I²C (up to 3.4MHz), SMBUS/PMBUS, SPI, LIN, UART and analog interfaces like: 12-bit, 1Msps ADC, Two Analog Comparators, Peripheral Touch Controller with capacitive touch and proximity sensing I/O